

Our Ref. No.: 042390.P5769

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Gang Bai

Application No.: 09/109,261

Filed: June 30, 1998

For: A MULTI-LAYER GATE DIELECTRIC

Examiner: Warren, Matthew E.

Art Unit: 2815

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OCT 05 2007

BOARD OF PATENT APPEALS
AND INTERFERENCESREPLY BRIEF

Mail Stop Appeal Brief - Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In the Appeal Brief filed November 2, 2005, Applicant argued that claims 8-10, 13-17 and 20-21 were not obvious over Nagata in view of Momose and Moon. Specifically, Applicant argued that the combined teachings of the cited references do not describe a transistor device having a gate electrode overlying a gate dielectric formed on a semiconductor substrate comprising a first dielectric material and a second dielectric material being scalable for a set of feature size technologies defined by a gate length in the range of 25-70 nanometers, where the first material thickness and the second material thickness are determined by the following relationship:

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox} \quad (4)$$

The Patent Office relied on Nagata to show the relationship of Equation (4). However, Applicant illustrated that the relationship shown in Nagata, where silicon dioxide is taught to be one of the dielectric materials, is as follows:

$$\begin{aligned}
 \frac{T_{eff}}{E_{SiO_2}} &= \frac{T_{SiO_2}}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \dots + \frac{T_{xi}}{E_{xi}} + \dots + \frac{T_{xn}}{E_{xn}} \\
 \frac{T_{eff}}{E_{SiO_2}} - \frac{T_{SiO_2}}{E_{SiO_2}} &= \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \dots + \frac{T_{xi}}{E_{xi}} + \dots + \frac{T_{xn}}{E_{xn}} \\
 \frac{T_{eff} - T_{SiO_2}}{E_{SiO_2}} &= \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \dots + \frac{T_{xi}}{E_{xi}} + \dots + \frac{T_{xn}}{E_{xn}}
 \end{aligned}
 \tag{5}$$

It is clear, that Equation (4) and Equation (5) are not identical. The Patent Office seeks to make them identical by ignoring silicon dioxide as one of the materials of Nagata. However, Nagata specifically teaches silicon dioxide as the dielectric material. In fact, the Patent Office must use Applicant's disclosure to get to Applicant's equation. See Examiner's Answer, p. 7. Applicant also notes that Momose, cited for its reputation of the feature size limitation of the claims, teaches only "gate oxide" (i.e., silicon dioxide) as its gate material. Moon, however, may describe itrium oxide (Y_2O_3) in connection with the ceramic material (e.g., PZT). Moon does not disclose a particular relationship between the Y_2O_3 and ceramic material relative to a particular thickness for a gate dielectric silicon dioxide.

For the above stated reasons, claims 8-10, 13-17 and 20-21 are not obvious over the cited references. Applicant respectfully requests that the Patent Office withdraw the rejection under 35 U.S.C. §103(a).

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Patent Office believes that a telephone conference would be useful in moving the application forward to allowance, the Patent Office is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 4/10/06

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nedy Calderon
Nedy Calderon

4/10/06
Date

TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>		Application No.	09/109,261
		Filing Date	June 30, 1998
		First Named Inventor	Gang Bai
		Art Unit	2815
		Examiner Name	Warren, Matthew E.
Total Number of Pages in This Submission	7	Attorney Docket Number	42390P5769

ENCLOSURES (check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Response <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> PTO/SB/08 <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Basic Filing Fee <input type="checkbox"/> Declaration/POA <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input checked="" type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): <div style="border: 1px solid black; padding: 5px; margin-top: 10px;">Return receipt postcard</div>
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	William Thomas Babbitt, Reg. No. 39,591 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	<i>William T. Babbitt</i>
Date	April 10, 2006

CERTIFICATE OF MAILING/TRANSMISSION			
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Typed or printed name	Nedy Calderon		
Signature	<i>Nedy Calderon</i>	Date	April 10, 2006

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT	(\$)	0.00
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Application Number	09/109,261
Filing Date	June 30, 1998
First Named Inventor	Gang Bai
Examiner Name	Warren, Matthew E.
Art Unit	2815
Attorney Docket No.	42390PS769

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20. ☒ Credit any overpayments

**or number previously paid, if greater. For Reissues, see below*

(S)

Date	04/10/06
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Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zeffman (wtr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Application No.: 09/109,281 Filing Date: 6/30/1998 Docket #: 42390.P5769
Date Mailed: 04/10/2006 Due Date(s): 04/10/2006
Client: INTEL CORPORATION Atty/Sec: WTB/ndc
Title: A MULTI-LAYER GATE DIELECTRIC

First Named Inventor: Gang Bai

The following has been received in the U.S.P.T.O. on the date stamped hereon:

Certificate of Mailing
Fee Transmittal (original & copy)
Reply Brief (3 pgs)
Transmittal Letter
Postcard

Assignee: Intel Corporation